Multi-objective Intrinsic Evolution of Embedded Systems

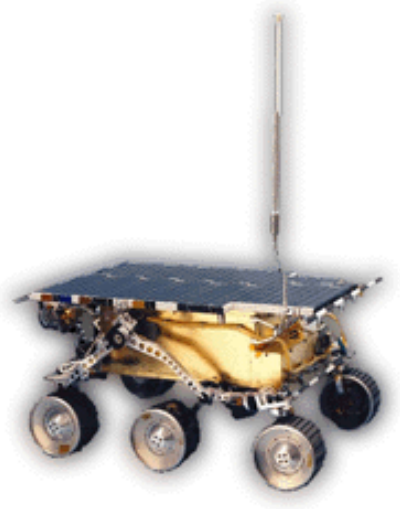
Marco Platzner
Computer Engineering Group
University of Paderborn

platzner@upb.de

UNIVERSITÄT PADERBORN
Die Universität der Informationsgesellschaft

Goal / Vision

- investigate intrinsic evolution as a mechanism to achieve self-adaption and –optimization for autonomous embedded systems

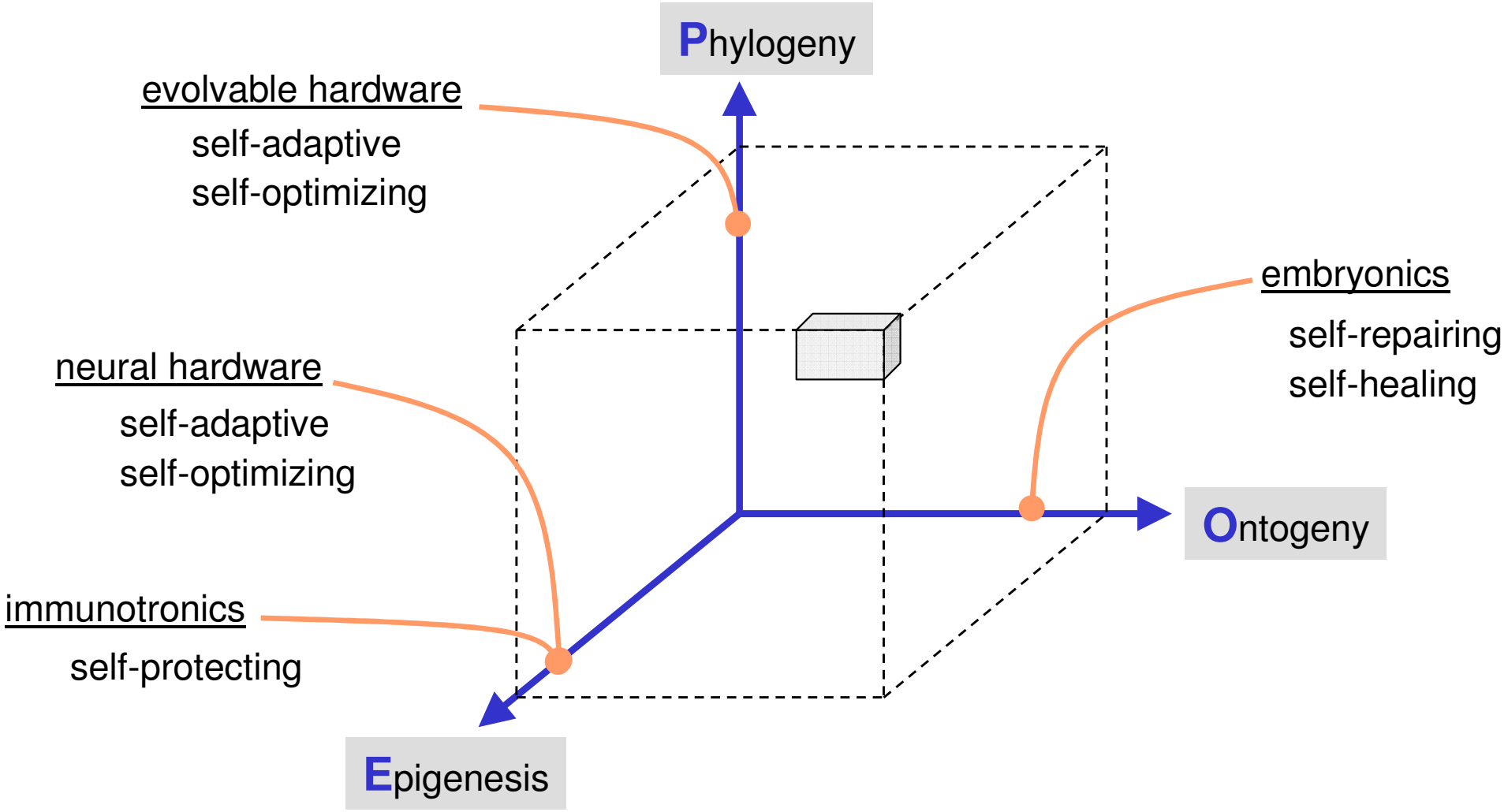


- an embedded system ...
  - adapts to slow changes by simulated evolution
    - typically, change of environment
  - adapts to radical changes by switching to pre-evolved alternatives
    - typically, change in computational resources
  - requires intrinsic evolution for autonomous operation

Outline

- goal / vision
- background
- work program
- potential collaboration areas

Biologically-inspired Hardware Systems



POE model [Sipper+97]

Evolvable Hardware (EHW)

- evolutionary algorithms applied at the hardware-level
  - term first used in [deGaris93, Higuchi+93]
- evolutionary algorithms are
  - population-based, stochastic optimization methods based on
  - biologically-inspired operators: selection, crossover, mutation
- hardware-level
  - digital or analog hardware, reconfigurable hardware is a good match
    - field-programmable gate arrays (FPGA)
    - field-programmable analog arrays (FPAAs)
  - the evolved circuit can be represented at various levels of abstraction
    - behavioral description (eg. VHDL program)
    - functional level (eg. dataflow graph)
    - gate level
    - bitstream for FPGA/FPAA

EHW – Fitness Evaluation

versus

extrinsic evolution

- fitness of a circuit is evaluated by a circuit simulator
- slow, used by most related work

intrinsic evolution

- fitness of a circuit is evaluated on the target system
- fast, fitness can include parameters of the real circuit

versus

off-line evolution

- use training data set to evolve the circuit, sometimes test data set to verify

on-line evolution

- circuit evolved while being operational, no training phase, no test data

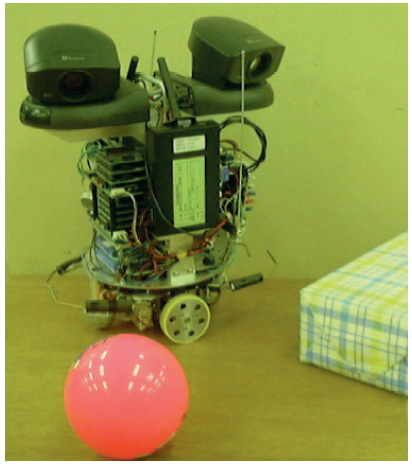
EHW – Time-varying Specifications

- embedded evolutionary circuit design {intrinsic, off-line}
  - eg. prosthetic hand controller [Higuchi+99-1]
  - specification changes rarely (changes in the biosignals of the arm)

- self-adaptive systems {intrinsic, off-line}
  - eg. real-time image processing, hashing [Damiani+98]
  - re-evolution triggered by a threshold on some parameter

- self-triggered systems {intrinsic, off-line}
  - eg. image compression by prediction coding [Sakanashi+04]
  - each block of input data triggers re-evolution

- on-line evolution {intrinsic, on-line}
  - eg. navigation and tracking for autonomously moving robots [Higuchi+99-1, Tyrrell+04]
  - problem: how to evaluate fitness?



classification according to [Sekanina04]

EHW – State & Challenges

- state of evolvable hardware
  - evolutionary circuit design: some astonishing circuits have been evolved, sometimes totally different from classically engineered circuits, sometimes even superior
  - time-varying specifications: first results demonstrate potential for self-adaption

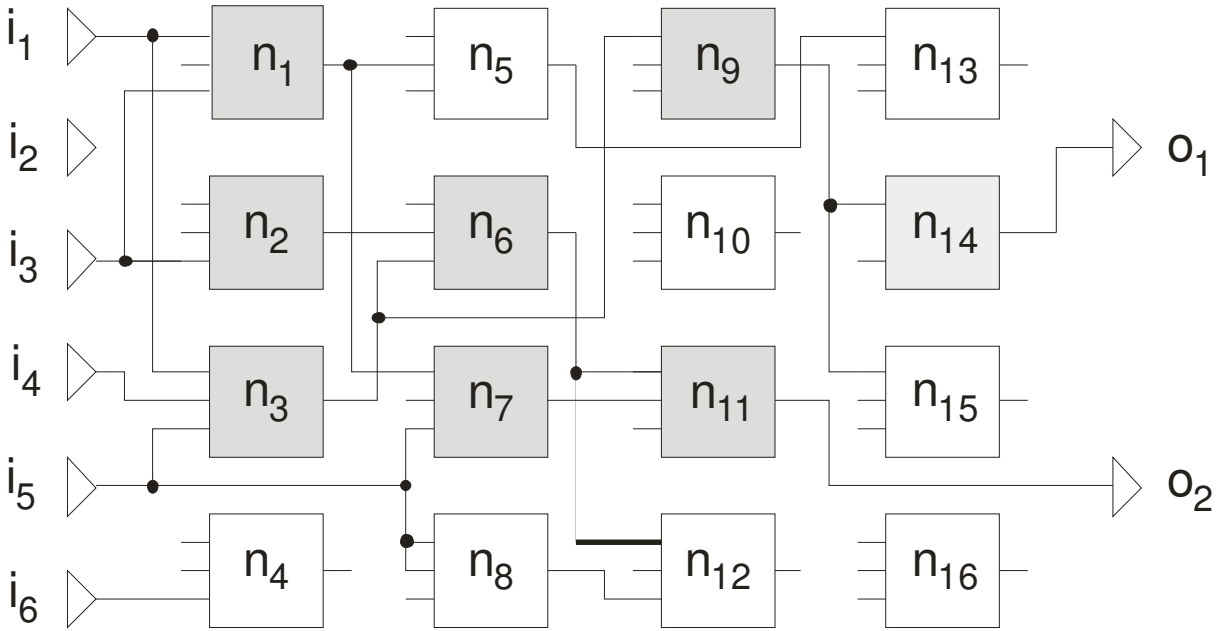
- main challenges in evolvable hardware
  - scalability: runtime does not scale with circuit size
  - robustness: unconstrained intrinsic evolution may produce circuits that are not useful from an engineering perspective
  - validation: evolution does not necessarily produce correct circuits

Work Program (Period I)

- investigate and develop models and algorithms
  - representation model for hardware/software functions
  - intrinsic multi-objective evolutionary algorithm
- develop basic hardware/software system architecture
  - self-reconfiguration
  - mapping to hardware and software
- analysis and evaluation
  - investigate application domains for intrinsic evolution, off-line and on-line
  - evaluate algorithms

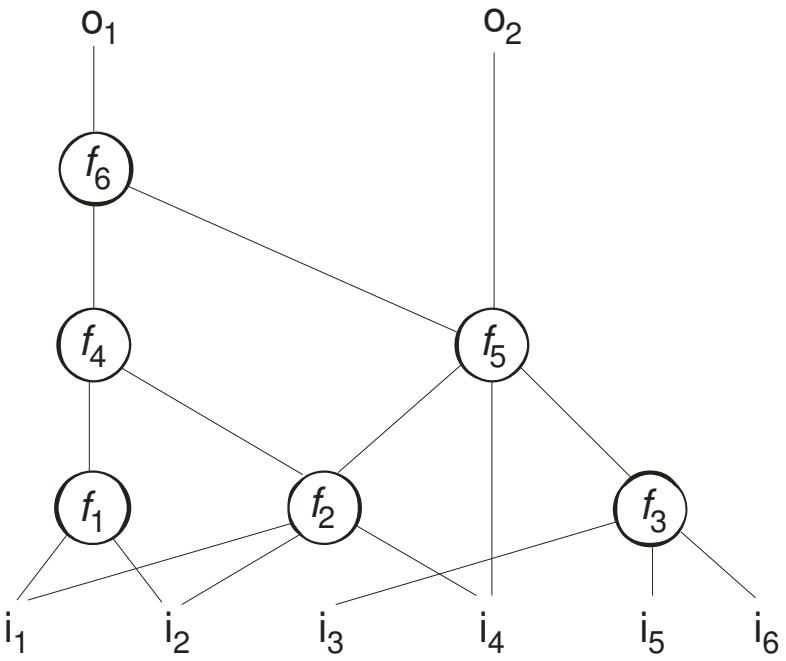
Hw/Sw Representation Model

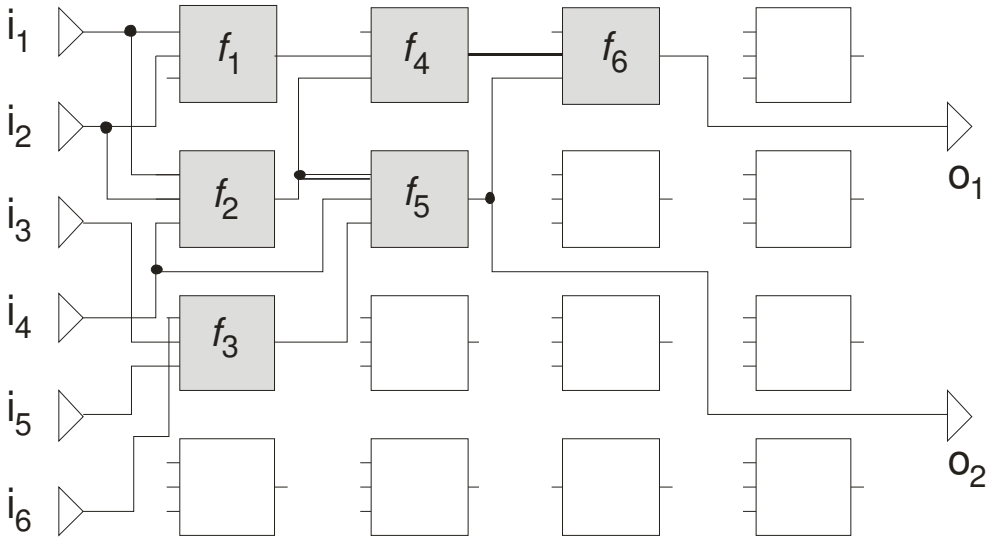
- encoding of circuits
  - compact to allow for efficient genetic operators
  - not too far away from real hardware to allow for efficient mapping
- cartesian genetic programming
  - matches FPGA architectures
  - unused blocks, unconnected inputs, redundant nodes



Hw/Sw Representation Model

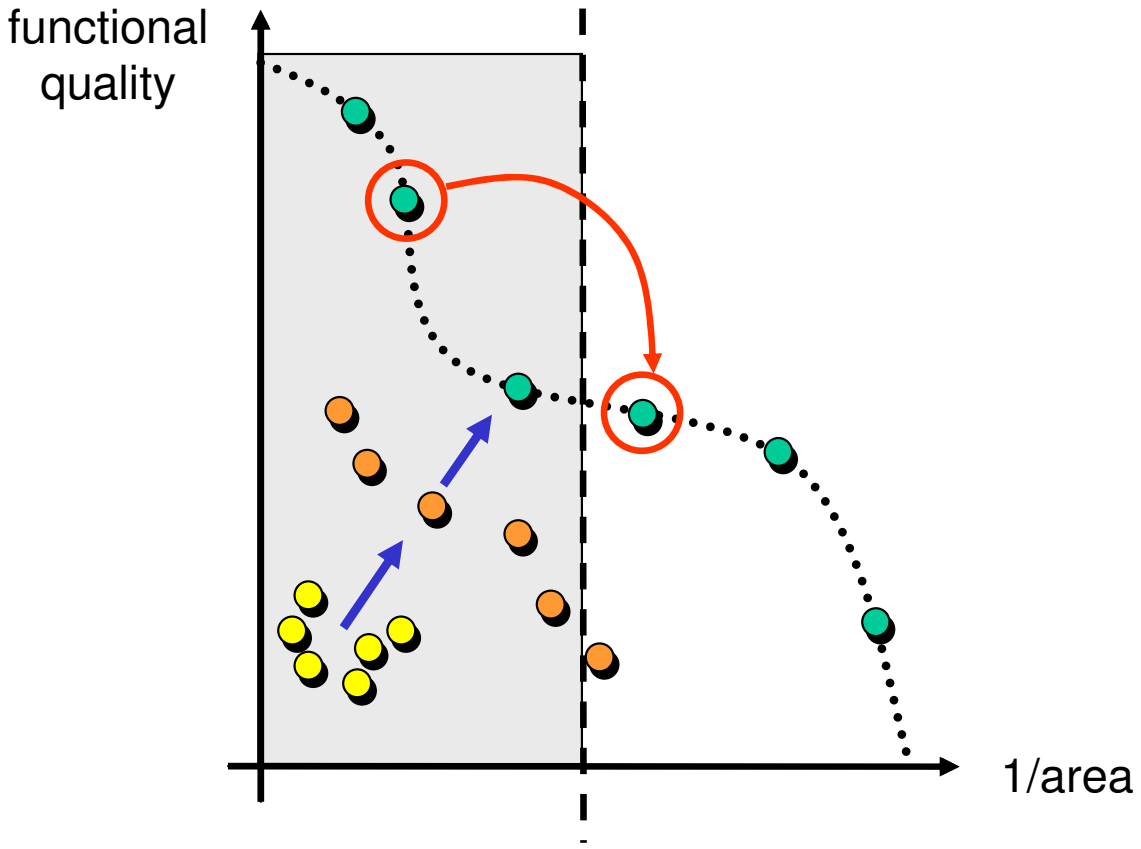
- approach: two-level representation
  - behavioral model allows for efficient genetic operators
  - structural model allows for efficient mapping to hardware and software
  - restrict behavioral model to simplify the transformation behavioral → structural





behavioral → structural

Intrinsic Multi-objective Evolutionary Algorithm



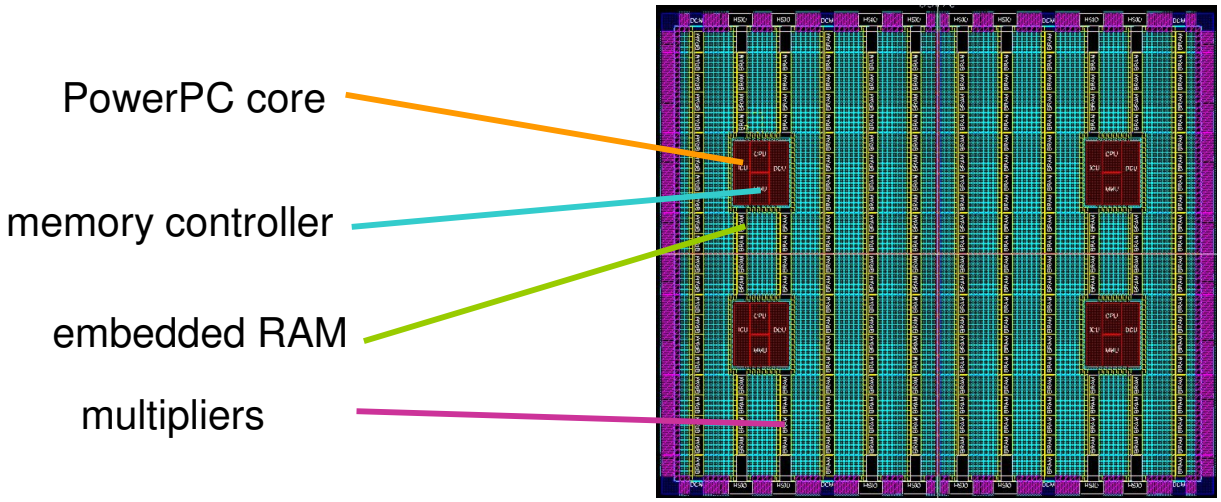
adapt to slow changes by simulated evolution

approximated Pareto front (functional quality, area, speed, energy)

adapt to radical changes by switching to pre-evolved alternatives

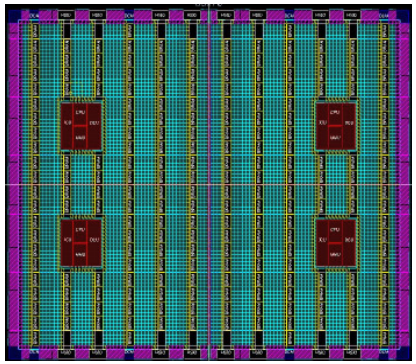
System Architecture and Application Analysis

- system architecture
  - Xilinx VirtexII Pro/Virtex-4 FPGAs as platform
  - partial reconfiguration



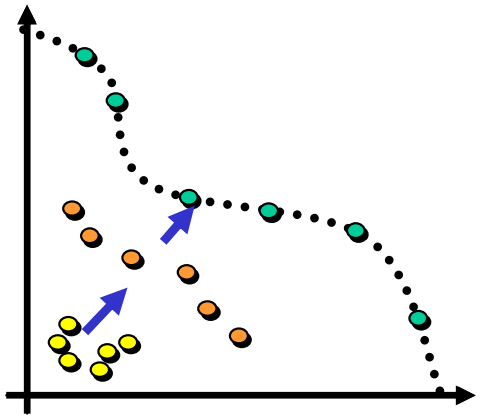
- application domain analysis
  - approach: functions that are characterized by some "functional quality" (rather than a binary correctness)
  - identify basic building blocks and interconnect structures for evolution

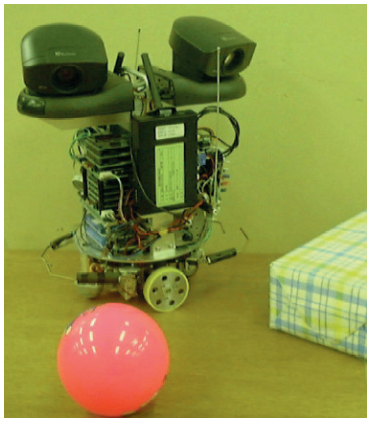
Potential Collaboration Areas



- architectures: "organic" systems-on-chip

- evolutionary algorithms: dynamic fitness functions





- applications: robotics, image compression

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